A 1~1.5 GHz Capacitive Coupled Inductor-less Multi-ring Oscillator with Improved Phase Noise

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***Abstract*—This paper presents a multi-ring coupled oscillator design that employs the common-source capacitive coupling technique to achieve improved phase noise by minimizing noise injection from tail current and adjacent rings. The proposed inductor-less ring oscillator also provides additional output phases for low noise multiphase clock generation. Implemented in a 130 nm CMOS technology, the 1.5 GHz triple-ring coupled ring oscillator achieved measured phase noise of -110.17 dBc/Hz @ 1 MHz offset, demonstrating 7 dB phase noise reduction comparing to its single-ring oscillator counterpart.**

I. INTRODUCTION

Multi-phase clock generation is critical for emerging technologies such as phase array, beam forming, passive mixing, N-path filtering and interleaved data converters. Multi-phase signal can be generated by ring oscillators with either resistive load or LC based delay cells. However, ring oscillators without LC tanks normally end up with unacceptable phase noise for most of the wireless applications. Thus, it is highly desirable for low cost applications to push the phase noise of ring oscillators close to what LC-based oscillators can reach. Recent researches on ring VCO showed phase noise improvement due to enhanced supply noise rejection by using multi-loop ring oscillator [1]. N path filters are also used to enhance the equivalent quality factor of the ring for improved oscillator phase noise [2]. Cyclic coupled ring oscillator uses inverter matrices to improve the phase noise by approximate$10\log_{10}(N_{RO})$dB through increased power consumption [3], where N_{RO} is the number of rings.

In this paper, we propose a multi-ring oscillator (MRO) that couples multiple rings with proper phase shifting to achieve phase noise improvement greater than $10\log_{10}(N_{RO})$ dB, leading to better Figure of Merit (FoM) than its single ring (SRO) counterpart. As shown in [4], common source coupling benefits from reduction of current tail noise. In addition, introducing phase delays in the coupling paths minimizes noise coupled from the adjacent cores [5]. The overall effect leads to improved phase noise performance as demonstrated in quadrature VCO designs [4] [5]. We applied this coupling technique to ring oscillator designs and implemented a triple ring coupled ring oscillator (TRO) with phase noise improvement of 7 dB at 1.5 GHz. It also triples the number of output phases compared to its single ring oscillator counterpart.

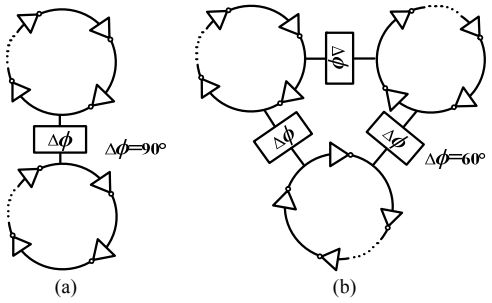

Fig. 1. Conceptual drawings of (a) double ring coupled ring oscillator (DRO) and (b) triple ring coupled ring oscillator (TRO).

II. ARCHITECTURE OF MULTI-RING OSCILLATOR

Ring oscillators comprise of multiple delay stages connected in a ring configuration. In order to operate at high frequency with large numbers of available output phases, more delay stages are required. However, this will lead to reduced oscillation frequency or increased power consumption to reduce delays between each stage. Under a given power consumption, the higher the oscillation frequency is and the more output phases are, the worse the phase noise becomes. This dilemma can be solved by splitting the delay stages into multiple rings and allowing each ring to oscillate at a higher frequency, yet still maintaining correlated phase relationship through coupling. Due to capacitive coupling, the proposed multi-ring oscillator which operates at higher frequency can achieve better FoM compared to the single ring with the same total number of delay stages. The coupling of additional rings turns out to be critical to the overall phase noise improvement. If proper phase shifting is introduced through the coupling, noise generated in the adjacent rings will be injected at the peak swing of the oscillation waveform in the main ring, where it is the least sensitive instance affecting the phase noise performance. If capacitive coupling is done at the virtual ground of the differential delay stages, i.e., common source coupling, additional phase noise improvement benefits can be obtained through tail current noise reduction. Hence, the proposed multi-ring coupled oscillator breaks the tradeoff between the number of phases and the oscillation frequency while gaining benefit from phase noise reduction.

As illustrated in Fig. 1 (a), a double ring coupled ring oscillator (DRO) is formed by connecting two ring oscillators through capacitive coupled paths with 90° phase shifting. Similarly, a TRO can be constructed by connecting three ring

oscillators through capacitive coupled paths with 60° phase shifting, as shown in Fig. 1 (b). This ensures that the noise coupled from the adjacent rings is not injected at the sensitive instances for phase noise performance.

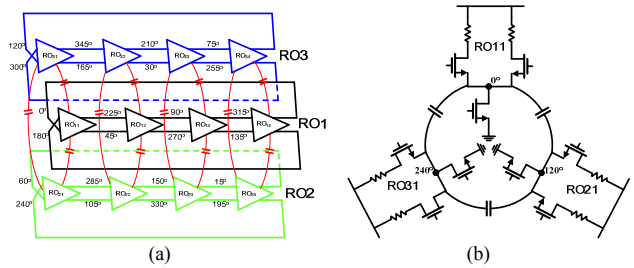

Fig. 2. (a) Block diagram and (b) simplified circuit diagram of the proposed triple ring coupled ring oscillator (TRO).

The proposed multi-ring oscillator (MRO) is further illustrated with block and circuit diagrams in Fig. 2. Three identical rings are implemented with 4 delay cells per ring. The ring oscillator is implemented with differential delay cells with resistive load shown in Fig. 2 (b). For comparison, the structure can be reconfigured as a SRO, a DRO and a TRO when one ring, two rings and three rings are powered on, respectively. The coupling between the rings is accomplished by connecting the virtual ground of the delay stages with capacitors. This common-source coupling scheme has two advantages: (i) the capacitive coupling provides needed phase shifting that minimizes the noise injection from the adjacent rings; (ii) the coupling capacitors provide phase shifting that minimizes the $1/f$ noise up-conversion generated by the current sources. As a result, the overall phase noise obtained from the TRO is greatly improved compared with its SRO counterpart. Note that the proposed capacitive coupling does not use any additional active devices, which add extra noise and power, nor does the coupling devices load any output nodes of the delay stages. Due to Miller effect, loading output nodes of a differential pair would limit the frequency response of the delay cells. Common-source coupling has ignorable effects on the oscillator's frequency response, yet it phase-shifts the signal injected from an adjacent ring. Thus, it helps the phase noise reduction without extra power and added noise. Since the 2nd harmonics are coupled, the phase relationship at the virtual grounds of three rings are forced to be 0°, 120°, and 240°, respectively. As a result, the overall available output phases are extended three times, namely, the 1st ring covers 0°, 45°, 90° and 135°, as well as their anti-phases 180°, 225°, 270° and 315°, while the 2nd and 3rd rings cover other 16 phases starting at 60° and 120°, respectively, shown in Fig. 1 (a).

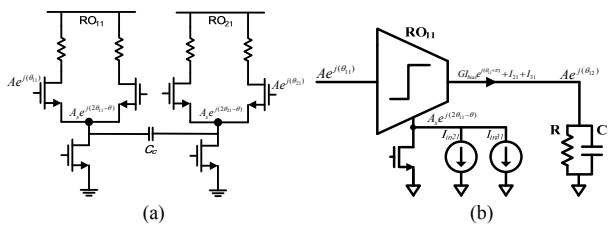

Fig. 3. (a) Simplified circuit diagram of DRO and (b) equivalent circuit model of delay cell RO11 for coupling and phase noise analyses.

The output frequency of the proposed MRO is determined by the total amount of delay experienced in a SRO, while the coupling scheme between the rings ensures their relative phase relationship. Assuming the MRO contains M rings with N delay cells per ring, the available output phases are $\varphi_{m,k} = \pi \cdot \left(\frac{m}{\mathrm{M}} + \frac{2n}{\mathrm{N}}\right), m = 0,1,\ldots,\mathrm{M}-1, n = 0,1,\ldots,\mathrm{N}-1$. Note that output phases may be overlapped for some combinations of M and N, e.g., the DRO case with 4 delay cells per ring. However, the proposed TRO with 3 rings and 4 delay cells per ring provides 24 non-overlapped multi-phase outputs. In addition, the increase of output phases does not come with penalty of reduced oscillation frequency, as the conventional SRO would suffer. Thus, high oscillation frequency and large numbers of output phases can be achieved simultaneously. It should be pointed out that the proposed MRO is not equivalent to duplicating rings and coupling them in-phase, which will not produce any additional output phases, nor will it the subtle noise reduction brought by the proposed multi-ring coupled structure.

III. Stability and Phase Noise Analysis

In this section, we present a theoretical model for the stability and phase noise analyses of the proposed multi-ring coupled oscillators. We first investigate the stability of possible steady state solutions, followed by phase noise analysis for the DRO by referring the injection currents and noise sources to the oscillator's output. Similar approach will be employed to derive the phase noise formula for the TRO. Theoretical analysis shows that compared to its SRO counterpart, the proposed DRO and TRO can lead to 5 and 7 dB phase noise improvement, respectively. Furthermore, the additional phase noise reduction can be obtained by shaping the tail current and varying the delay from source-to-gate voltage in the differential delay cells.

We assume all the delay cells operate as ideal hard limiting trans-conductors. In Fig. 3 (b), the single-end model of delay cell RO_{11} is used to perform stability and phase noise analyses in a DRO. For a delay cell RO_{mn}, the voltage signal coming from the previous delay stage is expressed as $Ae^{j(\theta_{mn})}$, where θ_{mn} and A denote its phase and magnitude; m represents its ring number index and n denotes its cell number index. The common source voltage $A_s e^{j(2\theta_{mn}-\theta)}$ of the delay cell RO_{mn} is the second harmonic of the input voltage $Ae^{j(\theta_{mn})}$ with certain gate-to-source delay θ and adjusted amplitude A_s. For quadrature operation, the phase difference φ between θ_{21} and θ_{11} can be written as $\theta_{21} - \theta_{11} = \frac{\pi}{2} + n\pi$, where $n = 0,1$. The two values of φ indicate that in the single ring, its phase distribution can be either clockwise or counter-clockwise. Note that two selected common source node voltages may be in phase and thus no current is injected from another core. This implies the case where two oscillators are free running without locking to each other. Such condition is a meta-stable state that has been proven unstable in [4]. Hence, only anti-phase case corresponds to a stable solution. By analyzing the voltage and current relation across the coupling capacitor C_C, we obtain

$$I_{in12} = C_C d(A_s e^{j(2\theta_{11}-\theta)} - A_s e^{j(2\theta_{21}-\theta)})/dt \quad (1)$$

Since $2\theta_{21}$ is the anti-phase of $2\theta_{12}$, the injected current I_{in12} from RO_{21} to RO_{11} can be expressed as $I_{in}e^{j2\theta_{21}+3\pi/2-\theta}$, where $I_{in} = 4C_c\omega_0 A_s$. The input oscillation waveform $Ae^{j\theta_{11}}$ up-converts the biasing current I_{bias} as $GI_{bias}e^{j(\theta_{11}+\pi)}$, while down-converts the injected current I_{in21}, as $I_{21} = GI_{in}e^{j(\theta_{21}+\varphi-\theta+\pi/2)}$, where G is the mixing conversion gain assuming a square switching waveform.

Writing KCL at the output node of the delay cell RO_{11} for DRO in Fig. 3 (b) yields

$$\frac{Ae^{j\theta_{12}}}{R} + C\frac{d(Ae^{j\theta_{12}})}{dt} = GI_{bias}e^{j(\theta_{11}+\pi)} + I_{21} \quad (2)$$

Solving the real and imaginary parts of (2), we have

$$\frac{d\theta_{12}}{dt} = \frac{1}{RC}\frac{I_{bias}\sin(\theta_{11}-\theta_{12})+I_{in}\sin(\theta_{21}+\varphi-\theta+\pi/2-\theta_{12})}{I_{bias}\cos(\theta_{11}-\theta_{12})+I_{in}\cos(\theta_{21}+\varphi-\theta+\pi/2-\theta_{12})} \quad (3)$$

where R and C is the load resistance and capacitance of single delay cell. Also we define parameters $\phi_0 = \theta_{11} - \theta_{12}$ and $\gamma_0 = \theta_{21} + \varphi - \theta + \pi/2 - \theta_{12} = \phi_0 - \theta + \pi/2$.

The coupling strength parameter M can be defined as the ratio between the injected current and biasing current, namely,

$$M = \left|\frac{I_{in}}{I_{bias}}\right| = \frac{4C_C\omega_0 A_S}{I_{bias}} \quad (4)$$

Using the similar approach given in [3], the generalized perturbation function A for all nodes in coupled oscillator can be derived using the primary matrix P and coupling matrix C as

$$A = \begin{bmatrix} P & C \\ C & P \end{bmatrix}_{8\times8}, \text{ with} \quad (5)$$

$$P = \begin{bmatrix} X+MY & 0 & 0 & -X \\ -X & X+MY & 0 & 0 \\ 0 & -X & X+MY & 0 \\ 0 & 0 & -X & X+MY \end{bmatrix} + j\omega_m RC \times I \quad (6)$$

$$C = -MY \times I \quad (7)$$

where $X = \frac{1+M\cos(\phi_0-\gamma_0)}{[\cos(\phi_0)+M\cos(\gamma_0)]^2}$, $Y = \frac{M+\cos(\phi_0-\gamma_0)}{[\cos(\phi_0)+M\cos(\gamma_0)]^2}$, and I is the 4×4 unit matrix. In above analysis, the offset frequency from carrier is set as ω_m= 1 MHz.

Solving the eigenvalues of the matrix A, we find that all the solutions are negative. This indicates all the possible states are stable. The phase noise at 1 MHz offset for a DRO can be derived as

$$L(\omega_m) = \frac{8kT}{R}\frac{(a^2+b^2)}{I_{bias}^2 b^4}\frac{1}{|det(P^2+C^2)|} \times [|PI|^2 + |CI|^2] \quad (8)$$

where T is absolute temperature, k is Boltzmann constant, and $a = \sin(\phi_0) + M\sin(\gamma_0),\ b = \cos(\phi_0) + M\cos(\gamma_0)$.

For a TRO, there are multiple possible stable states as well. The voltages of common source nodes are equally distributed by 2π/3 in phasor diagram. Following the similar approach used to solve the stability and phase noise in a DRO, we can prove that all possible states in a TRO are stable. For phase noise analysis, we combine the injection current vectors from RO 2 and RO 3 as a lumped injection current. This lumped injection current should have the same phase and magnitude as it has in a DRO. Thus, phase noise of a TRO at 1 MHz offset can be derived as

$$L(\omega_m) = \frac{8kT}{R}\frac{(a^2+b^2)}{I_{bias}^2 b^4}\frac{1}{|det(P^3+C^3)|} \times [|P^2I|^2 + |PC|^2 + |C^2I|^2] \quad (9)$$

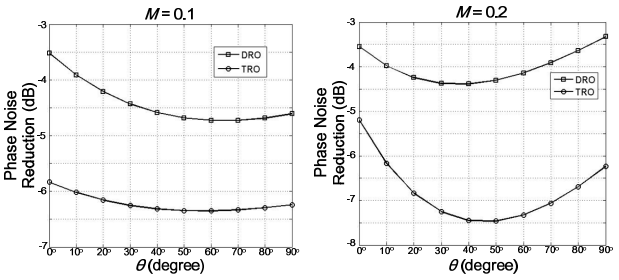

Fig. 4. Phase noise reduction compared to SRO versus gate-to-source phase delay θ with coupling factor of M=0.1 and 0.2.

In Fig. 4, we swept the gate-to-source delay θ under different coupling strength M=0.1, 0.2 and plot the phase noise at 1 MHz offset based on (8) and (9). It should be pointed out that the coupling strength, determined by the coupling capacitance C_C, affects gate-to-source delay θ. This further affects the phase noise and its corresponding optimal θ value. By properly sizing the coupling capacitor and the current source transistor, we can choose the optimal combination of θ and coupling factor M. For this particular design, we choose M=0.2 and θ=40°, and the simulation results show that it has about 7.4 dB phase noise improvement for a TRO and 4.4 dB improvement for a DRO compared to that obtained by a SRO. Furthermore, it also indicates that the phase noise improvement achieved by using DRO or TRO is greater than that by simply increasing the power in a SRO, where doubling or tripling the SRO power only improves phase noise by 3 dB or 5 dB, respectively, without adding additional output phases. The additional phase noise improvement is due to the optimal coupling that eliminates the noise injection from adjacent cells and by the reduction of current source noise up-conversion. The current injection from adjacent cells is shaped and moved away from the sensitive zero crossing instances. As a result, additional output phases and phase noise reduction are simultaneously achieved.

IV. Measurement Results

The proposed MRO RFIC was implemented in a 0.13 μm CMOS technology. The three rings RO1, RO2 and RO3 as well as their coupling capacitors P1, P2 and P3 are placed symmetrically with core area of 350×350 μm^2, as shown in Fig. 8. The ring oscillator circuits can be reconfigured as a SRO, a DRO or a TRO for comparison. Fig. 5 shows that the measured phase noise at 1.5 GHz output @ 1 MHz offset were -102.98, -106.97 and -110.17 dBc/Hz for the SRO, DRO and TRO, respectively. It demonstrates about 7 dB phase noise reduction when comparing the TRO with the SRO and 4 dB phase noise reduction when comparing the DRO with the SRO, agreed with our theoretical analysis. The output frequency of the MRO can be tuned from 1 to 1.5 GHz with the power consumption per ring ranging from 1.3 mW to 4.6 mW under a 1.2 V supply, respectively. Fig. 6 gives the measured phase noise @1MHz offset for the MROs across the frequency tuning range of 1~1.5GHz, in which phase noise improvement using the

proposed MRO technique has been clearly demonstrated. The performance summary and comparison table I demonstrates the effective phase noise reduction by the proposed MRO technique. Moreover, the tradeoff between power consumption and phase noise in the MROs has been further investigated with higher power consumption than what was designed. Under an increased 1.5 V power supply, it shows the measured phase noise performance of the TRO reaches -118 dBc/Hz at 1.8 GHz output as shown in Fig. 7, approaching the phase noise performance of LC-based oscillators. We expect reduced power consumption and improved FoM in advanced technologies with smaller feature sizes. Nevertheless, this work demonstrates an inductor-less ring oscillator with good phase noise performance when compared to state-of-the-art ring oscillator designs summarized in the comparison Table I. The FoM of the TRO reaches 162.3 dBc/Hz. When considering multi-phase outputs, the FoM per phase of the MRO reaches 176.1 dBc/Hz. Therefore, the proposed inductor-less MRO provides an effective means for high frequency, low phase noise and low cost multi-phase clock generations.

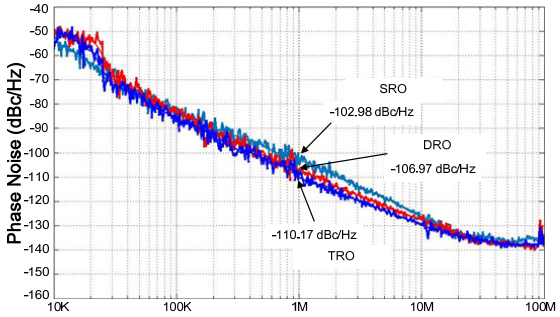

Fig. 5. Measured phase noise of SRO, DRO and TRO at 1.5GHz output.

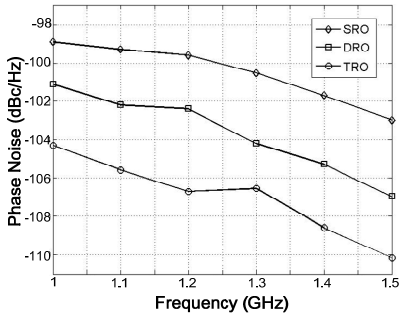

Fig. 6. Measured phase noise of MRO versus tuning frequency f_o.

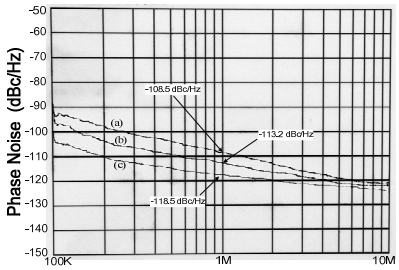

Fig. 7. Measured phase noise of SRO, DRO and TRO at 1.8GHz output.

V. Conculsions

A capacitive coupled inductor-less multi-ring oscillator is presented in the paper with improved phase noise and increased number of output phases. The common source coupling technique with proper phase delay minimizes the noise injection and the tail current shaping further reduces current source noise up-conversion, thus leading to greatly improved FoM per output phase. In addition, coupling through common source nodes doesn't load the signal path, allowing high frequency. The stability and phase noise of the proposed MRO circuits were analyzed and modeled. The effectiveness of the proposed technique was verified with a 1~1.5 GHz 24 phase TRO multi-ring oscillator fabricated in a 0.13 μm CMOS technology. The prototype achieved measured phase noise reduction of 7 dB compared to its SRO counterpart with PN @1MHz approaching -110.17 dBc/Hz and FoM reaching 162.3 dBc/Hz and FoM per phase reaching 176.1 dBc/Hz. Therefore, the proposed inductor-less MRO provides an effective means for high frequency, low phase noise and low cost multi-phase clock generations.

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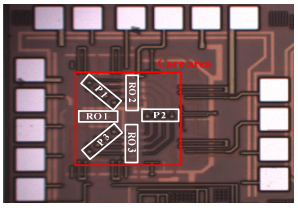

Fig. 8. Die photo of MRO RFIC.

TABLE I Performance Summary and Comparison

Architecture	This Work		[1]	[2]	[3]
	DRO	TRO	Multi-loop	N-Path	Cyclic
Technology	130 nm		90 nm	90 nm	90 nm
f_o range (GHz)	1.0~1.5		0.63~8.1	0.2~1.8	1~12.8
PN @ 1MHz (dBc/Hz), f_o	-107.0, 1.5GHz	-110.2, 1.5GHz	-106, 0.63GHz	-110, 1GHz	-105, 7.7GHz
Power (mW)	2.6~9.2	3.9~13.8	7~26	4.7	13~200
Output phases	8	24	4	6	3
FoM (dBc/Hz)	161	162	135	163	160
FoM per phase (FoM_P)(dBc/Hz)	170	176	141	171	165

$$\text{FoM} = 10\log\left[\left(\frac{f_o}{\Delta f}\right)^2 \frac{1\,\text{mW}}{P}\right] - L(\Delta f), \text{FoM}_\text{P} = \text{FoM} + 10\log(\text{No. of Phases})$$